Extrinsic and Intrinsic Charge Trapping at the Graphene/Ferroelectric Interface

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Recently, there have been several studies on integrating graphene with single crystal ferroelectric thin films like $Pb(Zr_xTi_1-x)O_3$ (PZT) [1–3] and (Ba,Sr)TiO_3 [4], with the aim of fabricating graphene ferroelectric field effect transistors (GFeFETs). Ferroelectric thin films, as a gate dielectric material, have high-κ values that can enhance the graphene channel carrier mobility [5]. Graphene, which acts as a screening material, can be used to read the switching of spontaneous polarization of the ferroelectric gate material, forming the basis for "non-volatile" memory applications [6].

In general, the characteristics of GFeFETs have been affected by anti-hysteresis associated with charge trapping. The cause has been attributed to water molecules [2] and large densities of H^+ and OH^- [1] ions that screen the ferroelectric polarization at the graphene/ferroelectric interface. More recently, the gating of graphene showing proper ferroelectric hysteresis, at room temperature, has been demonstrated by preserving the cleanliness of the graphene/PZT interface [7]. However, the hysteresis depended strongly on the ramping speed of the gate voltage indicating the presence of slow trapping processes, which are associated with surface adsorbates such as water molecules.

In this work [8], the problem of surface adsorbates was tackled by using artificially layered $PbTiO_3/SrTiO_3$ (PTO/STO) superlattices. A schematics of a GFeFET with PTO/STO as the gate dielectric is shown in Fig. 1 (a). The transition temperature and polarization of PTO/STO superlattices can be tuned by changing the PTO volume fraction [9]. Exfoliated graphene was deposited on the superlattice at 250°C, which can effectively decrease the ferroelectric polarization as much as 70%. With ideal superlattice growth conditions and extrinsic adsorbates largely removed, a direct coupling is seen between the graphene channel and the ferroelectric superlattice, as shown in Fig. 1 (b).

Polarization switching, indicated by the peaks of the C-V curve of the superlattice (Fig. 1 (d)), matches with the position of the graphene Dirac peaks as the gate voltage is swept between ±4V. For sub-hertz gate voltage ramping speeds, the dynamics of the Dirac peak positions are virtually unchanged, as shown in Fig. 1 (c). This is indicative of an absence of slow trapping processes, which were commonplace previously [7].

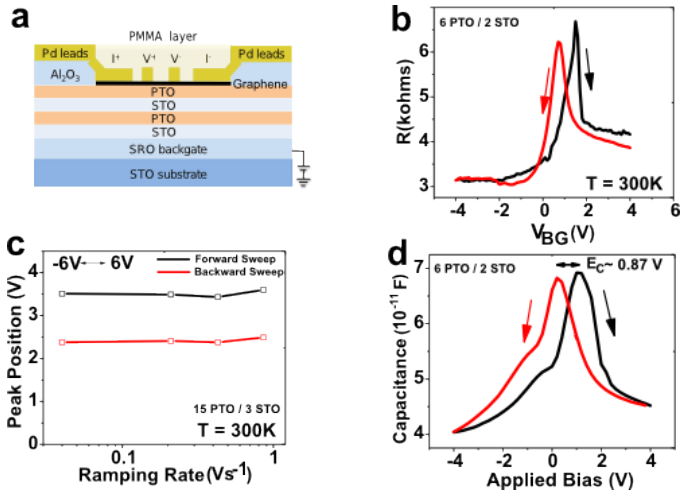

FIG. 1. (a) Schematics of a Graphene Ferroelectric Field Effect Transistor (GFeFET). (b) Graphene channel response due to ferroelectric domain switching at room temperature. (c) For sub-hertz frequencies, the graphene hysteresis is independent of gate ramping speed (d) The capacitance-voltage (C-V) characteristics of the PTO/STO superlattice shows a direct capacitive coupling between graphene and the ferroelectric gate.

With the removal of such extrinsic charge traps, the impact from the "intrinsic" defects of the ferroelectric substrate was revealed. The defects manifested themselves as antihysteresis on the graphene channel. However, this type of antihysteresis has several distinguishing characteristics:

1. The antihysteresis cannot be subdued at cryogenic temperatures (Fig. 2 (a)) as opposed to adsorbate-associated antihysteresis [4];

2. The antihystersis is caused by traps that preferentially trap more electrons than holes from the graphene channel, giving rise to an asymmetric trapping behavior;

3. Compared to the adsorbate-associated traps, the surface defect-associated intrinsic traps show much faster time-response ~10 μs (Fig. 2 (b)).

A systematic study was carried out to identify the source of such intrinsic charge traps and their impact on the switching behavior of the graphene field effect devices. It was found that the intrinsic traps are largely

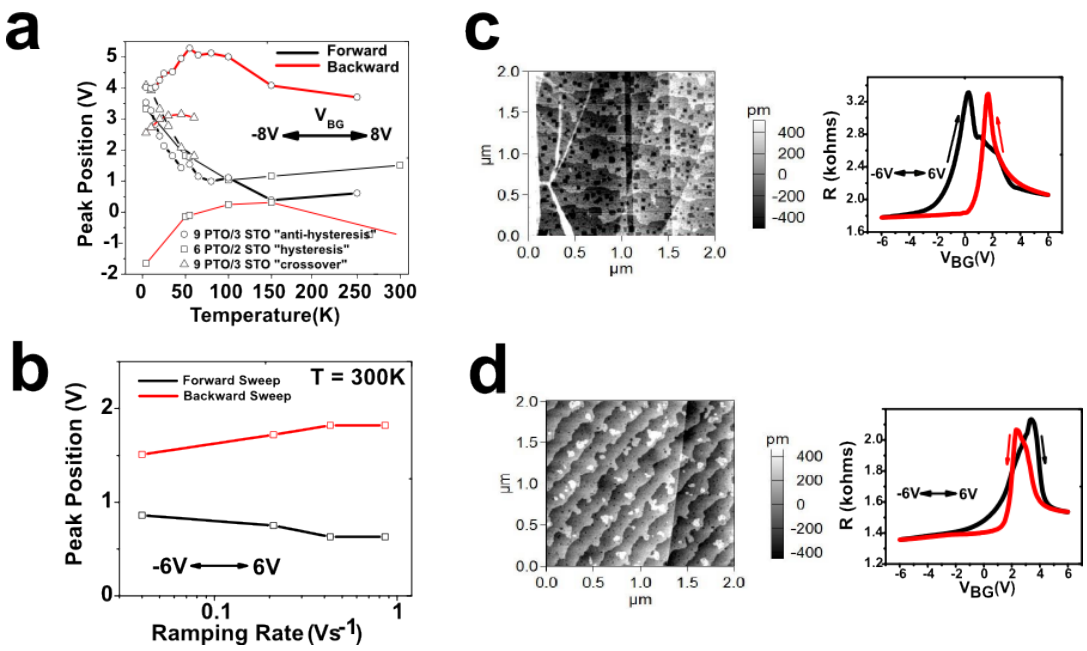

FIG. 2. (a) Dirac point peak position versus temperature for forward and reverse gating for various samples. Remarkably, the forward gate ramping peak positions (black curves) were qualitatively and quantitatively similar for all the devices. This indicates an asymmetry in electron and hole trapping. (b) For sub-hertz frequencies, the anti-hysteresis is robust. This indicates a fast trapping processes. (c) Defects on the ferroelectric surface facilitate charge trapping, and graphene demonstrates"anti-hysteresis". (d) An ideal interface restores ferroelectric switching on the graphene channel.

influenced by the growth parameters of the ferroelectric superlattices. Such intrinsic charge traps, while showing little impact on the C-V characteristics of the superlattice, strongly affect the resistance gating of the graphene channels. Comparing the surface topography of the devices with their gating curves (see Fig. 2 (c) & 2 (d)), the charge trapping centers were attributed to physical defects associated with the dangling bonds on the surface of the superlattice, which cannot be processed or removed simply by making the interface free of adsorbates. These defects manifest themselves as single atom deep, square shaped pits, which may be associated with the 1x6 surface reconstruction of $PbTiO_3$, associated with PbO deficiency [10].

These results are the first successful demonstration of robust, ramping speed independent, room temperature ferroelectric switching in GFeFETs. Through comparison with numerical simulations, a deeper understanding of the graphene-ferroelectric interface was established. This paves the way to reliably study graphene-ferroelectric hybrid devices, and to extend the work to other novel 2D atomic layer systems and ferroelectric systems. This work also established PTO/STO ferroelectric superlattice system as a suitable system for combining two dimensional atomic crystals (2DACs) with ferroelectricity.

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[1] X. Hong *et al.*, Appl. Phys. Lett. **97**, 033114 (2010).
[2] E.B. Song *et al.*, Appl. Phys. Lett. **99**, 042109 (2011).
[3] Y. Zheng *et al.*, Epl-Europhys. Lett. **93**, 17002 (2011).
[4] A. Rajapitmahuni *et al.*, Nano. Lett. **13**, 4374 (2013).
[5] X. Hong *et al.*, Solid State Commun. **152**, 1365 (2012).
[6] Y. Zheng *et al.*, Appl. Phys. Lett. **94**, 163505 (2009).
[7] C. Baeumer *et al.*, Nano. Lett. **13**, 1693 (2013).
[8] M.H. Yusuf *et al.*, Nano. Lett.**14**, 5437 (2014).
[9] M. Dawber *et al.*, Adv. Mater. **19**, 4153 (2007).
[10] A. Munkholm *et al.*, Phys. Rev. Lett. **88**, 016101 (2002).